TCAD Driven CAD

A Journal for Process and Device Engineers

FastATLAS
An Ultra-Fast Physical MESFET and HEMT Simulator

Introduction

By designing specifically for MESFETs and HEMTs Silvaco has optimized device simulation algorithms to produce a new and highly efficient simulation framework to be released as **FastATLAS.** Simulations with **FastATLAS** are typically 1000 to 10000 times faster than **ATLAS** allowing truly interactive TCAD. **FastATLAS** includes all the relevant physical models currently available within the **ATLAS** framework, maintaining simulation accuracy while delivering unprecedented speed.

FastATLAS and **ATLAS** were both used to simulate a 0.5 micron gate length recessed GaAs MESFET structure. The **ATLAS** structure contained 2700 nodes and averaged around 55 seconds per bias point on a SUN Sparc ULTRA workstation. The same structure was simulated with **FastATLAS** which automatically generated a mesh using over 15000 nodes yet reduced the simulation time to 7.5 milliseconds per bias point, a speed increase by a factor of 7000! **FastATLAS** timings for typical analyses are given in Figure 1.

FastAtLAS Simulation Timings

Type of Analysis	CPU Time on Sun SPARC 20
Charge Control analysis	24 seconds
DC Id/Vds family (drift-diffusion, 119 points)	2.6 seconds
DC Id/Vds family (energy balance, 99 points)	1.4 seconds
DC Id/Vgs sweep (energy balance, 21 points)	2.5 seconds
Rf rapid (energy balance, 33 points)	1.3 seconds
Rf full-period (energy balance, 128 points)	2.5 seconds
Rf swept - full period (energy balance, 7552 points)	59 seconds

Figure 1. All simulations were on a 0.5µm gate length recessed MESFET. The DC-IV simulations were taken over the range -2<Vgs<0, 0.5 volt increments, 0<Vds<5, 0.1 volt increments. The Id/Vgs sweep was taken over the range -2<Vgs<0, 0.1 volt increment Vds = 0.1 volts. The RF simulations were taken at the bias point Vgs = 0, Vds = 2 volts, freq = 20 GHz, and the RF swept simulation was taken at Vgs = 0, Vds = 2 volts 1<freq<30 GHz, 0.5 Ghz increment.

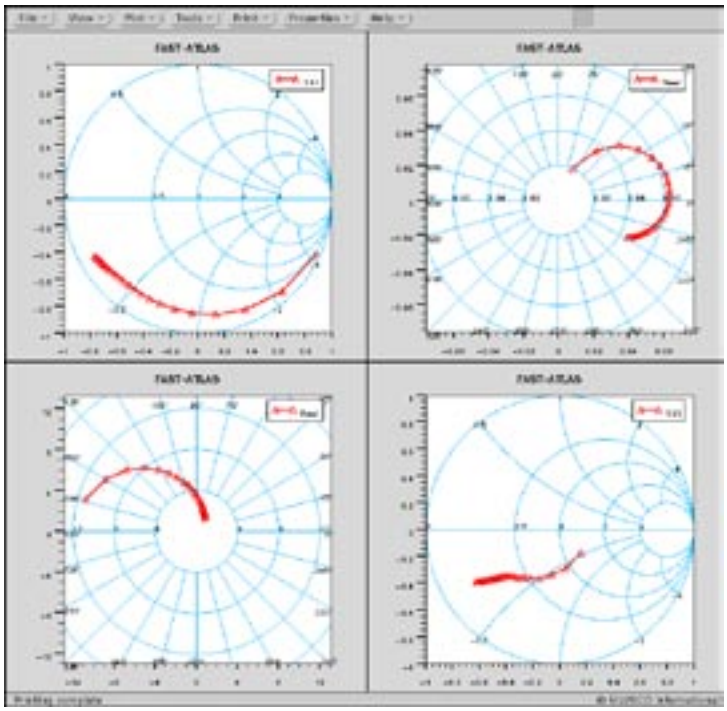

Figure 2. Small-signal RF simulaton of a GaAs/AlGaAs/ GaAs HEMT biased at 0 volts V_{GS}, 2 volts V_{DS}. Frequency sweeps from 1 Ghz to 25 GHz in 1GHz intervals.

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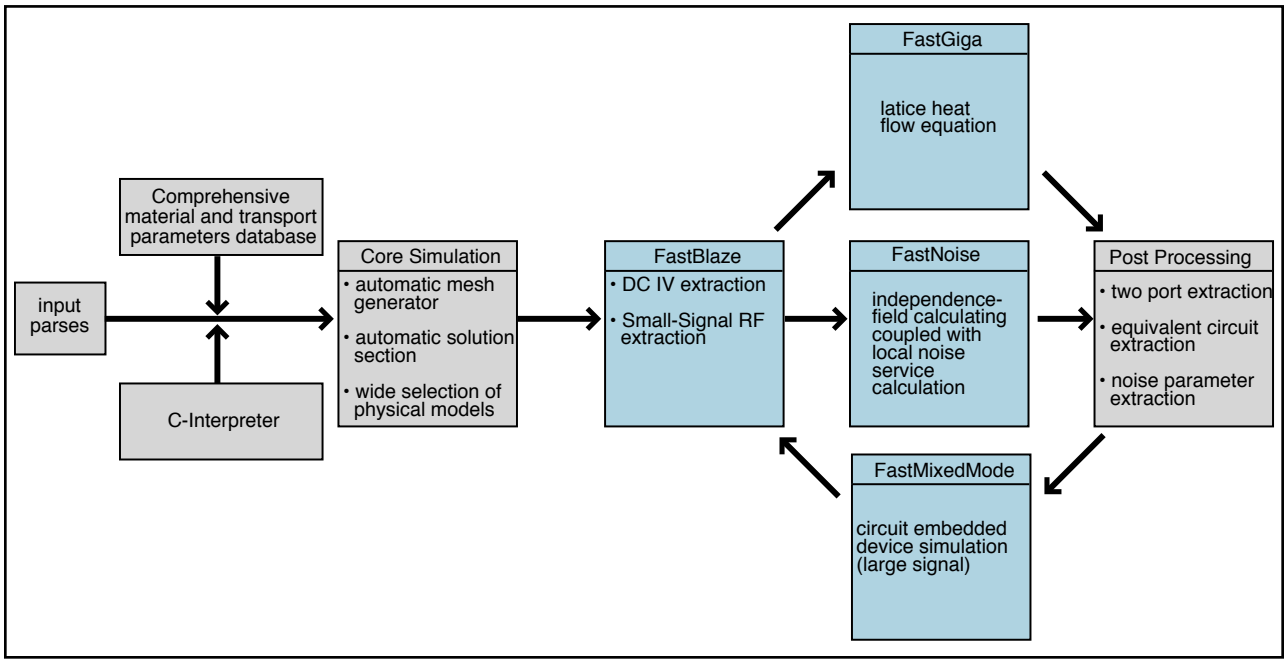

Figure 3. Architecture of **FastATLAS** framework.

FastATLAS Architecture

The complete suite of **FastATLAS** modules is illustrated in Figure 3. The core simulator incorporates the physical models present in **ATLAS** including complex effects such as energy-balance and velocity overshoot. These features are coupled with a comprehensive material parameter database, input parser, c-interpreter and several post-processing options including various two-port and equivalent circuit extraction algorithms. **FastATLAS** has been designed to be user friendly and includes several features to enable ease of use. One important development has been the inclusion of an automatic mesh generation algorithm, relieving the user from this arduous and time-consuming task. The speed of the simulation process enables **FastATLAS** to perform trial solutions using an exceptionally dense mesh, typically with only two Angstrom node spacing. The solutions are then analyzed and a non-uniform mesh generated that maintains solution accuracy and enables high simulation speed. A typical mesh generated by **FastATLAS** is shown in Figure 4, illustrating the clustering of nodes, especially at the drain edge of the gate. In addition the solution sequence has been automated. In **FastATLAS** it is not necessary to specify solution techniques since the simulation procedure automatically and robustly solves for all biases. Combining these features produce a flexible simulation tool able to rapidly characterize arbitrary FET structures.

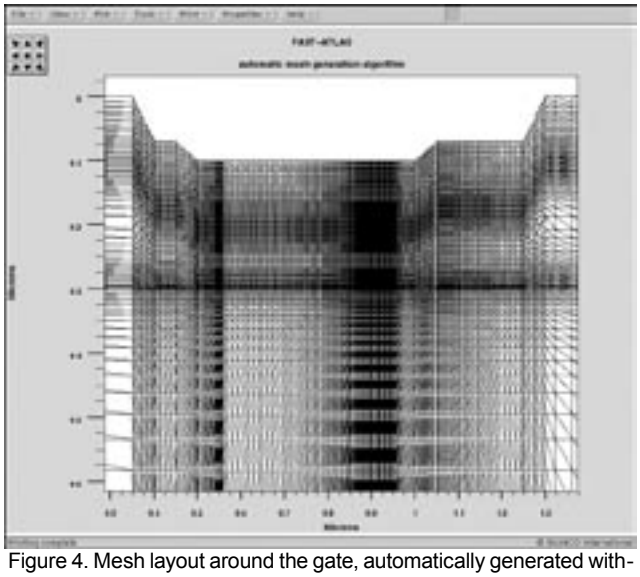

Figure 4. Mesh layout around the gate, automatically generated within **FastATLAS.** Typical mesh size at drain edge of gate 2.8 x 0.6nm.

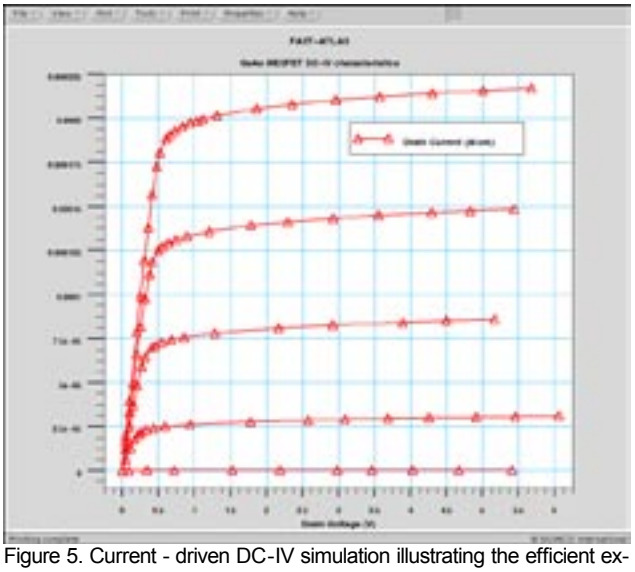

Figure 5. Current - driven DC-IV simulation illustrating the efficient extraction algorithm, where samples are only taken in regions of change.

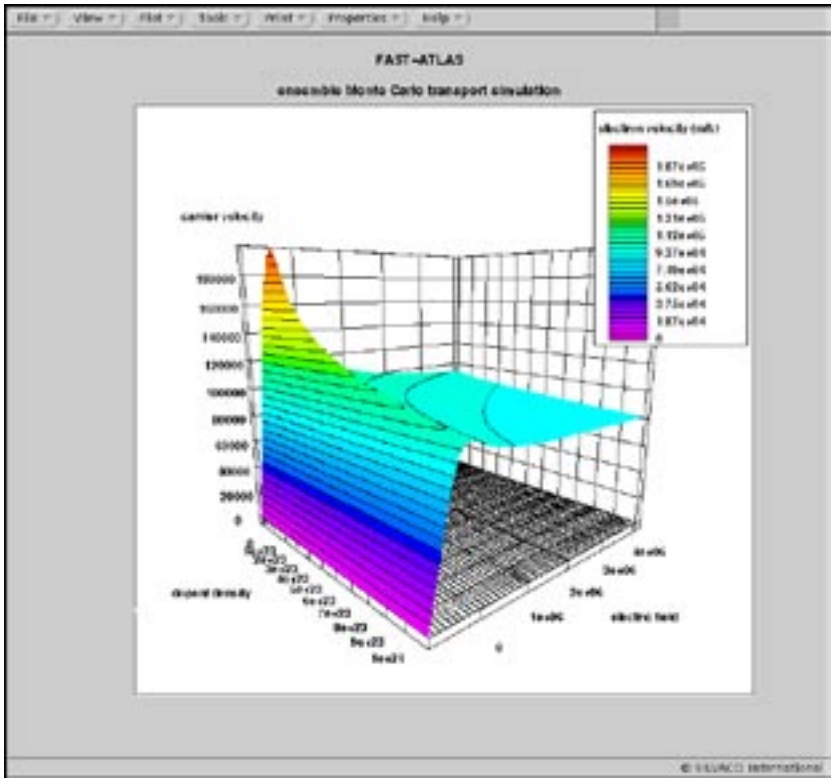

Figure 6. Carrier velocity as a function of electric field ($V.m^{-1}$) and doping density (m^{-3}). Generated using a 3 valley ensemble Monte Carlo model.

Module Description

FASTBlaze, is the simulator that solves DC single point and swept IV simulation and the small-signal time-domain RF single point and swept bias simulations. One of the benefits of an extremely fast simulation is that one can perform time-domain simulations. This is done within **FastATLAS** and forms the basis of the RF simulator. In the small-signal simulation sinusoid input signals are applied to the terminals and their effects monitored. The user can then select from time-domain or a variety of two-port output options.

FastGiga incorporates the lattice heat flow equations into **FastBlaze** accounting for thermal effects, particularly important in power applications. One new development is to include a comprehensive transport parameter database derived from an ensemble Monte Carlo simulation. The transport models implicitly include the effects of field, doping and importantly for **FastGiga,** lattice temperature.

FastNOISE is capable of extracting noise parameters for a simulated device. This simulation incorporates a variety of noise mechanisms and uses the impedance-field method to obtain the terminal characteristics. Again several post-processing options are available allowing **FastNOISE** to output the conventional noise parameters: F_{min}, R_n and Γ_{opt}.

FastMixedMode embeds any of the modules listed above within a circuit enabling the user to perform TCAD on complex systems of devices and passive elements. This feature leads to large-signal analysis which will include both time-domain and harmonic balance techniques.

Features

One method of the optimizations has been to modify the **ATLAS** code from a "voltage driven" format, where the terminal biases are applied, to a "mixed current/voltage driven" form, where the input (source) current and gate bias are specified and used to calculate the corresponding drain bias and gate current. This new approach allows **FastATLAS** to reduce simulation times by an order of magnitude. Unfortunately if a solu-

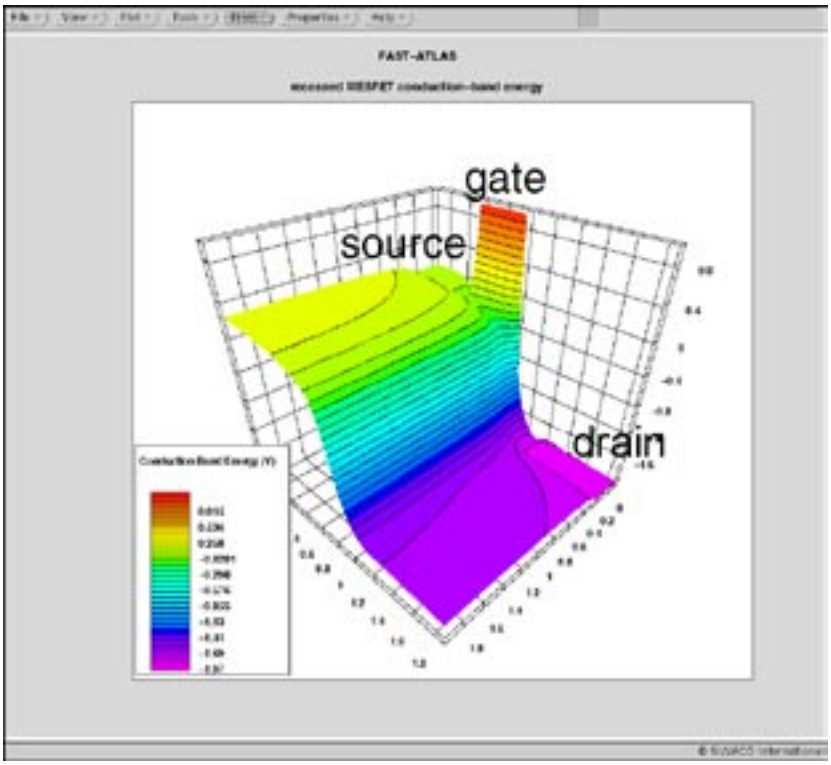

Figure 7. Conduction band profile generated by **FastATLAS** for a 1/2 micron gate MESFET biased at 2 volts V_{DS}.

tion at a specified drain bias is desired this must be found using ireation on the drain current, somewhat reducing the gains in efficiency. However, importantly, if a DC-IV sweep is performed the simulator can be left in "current-driven" mode and no iteration is necessary. In fact an automatic DC-IV generation algorithm has been written that increases the efficiency of the whole simulation since it is able take large steps in the linear regions of device operation and only refines the output in areas of change, in particular around the "knee" of the IV curve and at breakdown. The results can then be interpolated onto individual drain bias positions, with accuracy guaranteed by the tolerance entered into the generation algorithm. Typical results are displayed in Figure 5 illustrating the clustering around the knee and larger steps in the ohmic region of device operation and as the device goes into saturation. The interpolated results taken from this curve have less than 0.003% error compared with the full voltage-driven results and were completed in less than 4% of the time.

Transport options include conventional drift-diffusion and hydrodynamic energy balance, with a range of different mobility and energy relaxation models. An additional feature available in **FastATLAS** is the transport parameter database. A new set of models have been developed using three valley ensemble Monte Carlo simulation to derive the carrier mobility, velocity, effective mass and both the energy and momentum relaxation times as functions of electric field, doping and ambient lattice temperature. Figure 6 illustrates the variation of carrier velocity as a function of field and doping in GaAs where velocity overshoot and saturation are clearly visible. Further, due to the new automated solution process the simulation convergence is relatively independent of transport models. **FastATLAS** works within the VWF framework, and is interfaced to all SILVACO input and graphical analysis tools. Figure 7 displays the conduction band energy of a recessed GaAs MESFET biased at 2 volts Drain-Source, and volts on the gate.

Conclusion

FastATLAS is a new and highly efficient TCAD tool for arbitrary, non-planar MESFET and HEMT device simulation. New techniques allow automated mesh generation, bias step control and very high frequency analysis. Device optimization can be done using the most advanced physical model with almost no speed penalty. A 1000x to 10000x speed up over conventional device simulation allows results to be obtained in seconds.

3D Numerical Simulation of the Pseudo-MOS Transistor for SOI Film Characterization

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Introduction

The electrical characterization of SOI wafers is a difficult task due to the thinness of the film and complexity of the stacked structure. This is why the electrical properties are, in general inferred from the analysis of test MOS device or integrated circuits. Described below is a simple technique that takes advantage of the specific configuration of SOI and has the potential of being nondestructive. The pseudo-MOS transistor, also called the point-contact transistor or Ψ-MOSFET, is the first transistor that does not require any lithography or technology at all.

The Ψ-MOSFET is based on the inverted MOS structure that is inherent in all SOI materials. Figure 1 shows that the bulk-Si substrate can act as a gate terminal and can be biased to induce a conduction channel at the upper interface of the buried oxide.

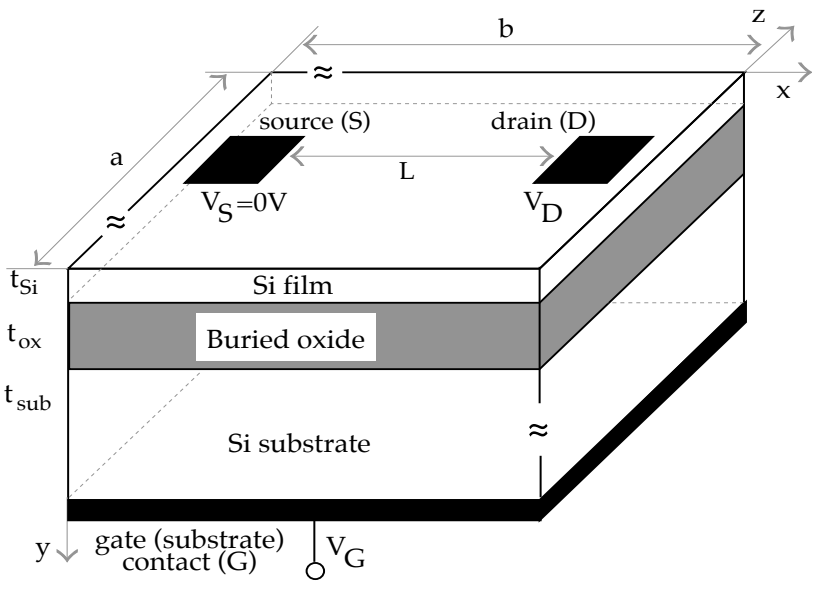

Figure 1. 3D structure used for simulation of Ψ-MOSFET.

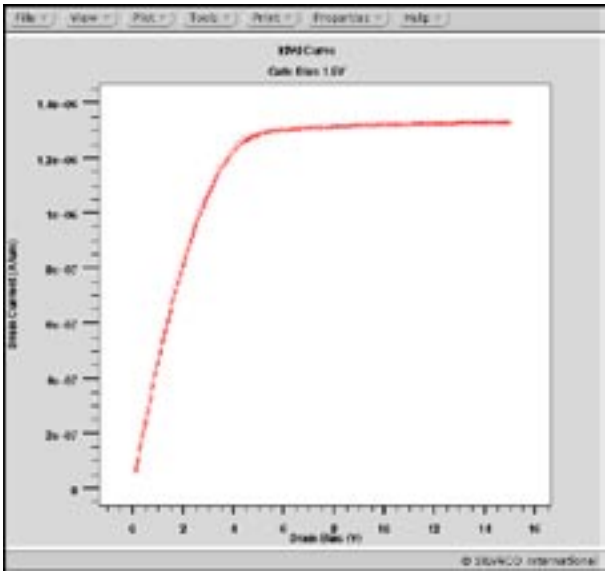

Figure 2. IdVd curve simulation of Ψ-MOSFET.

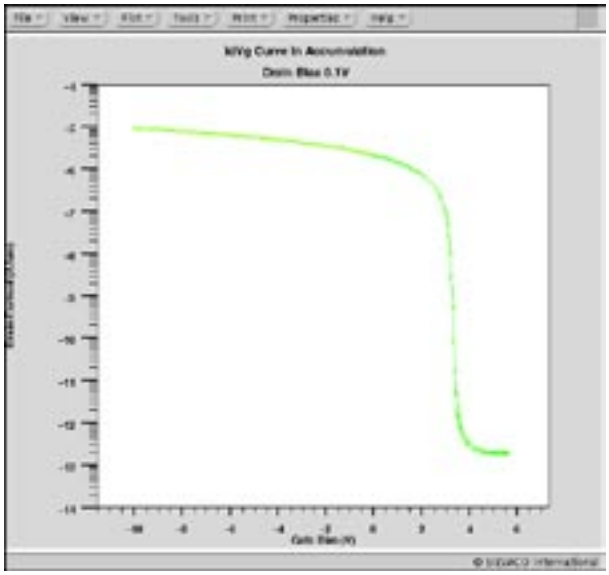

Figure 3. IdVg curve simulation of Ψ-MOSFET.

The buried oxide plays the role of a gate oxide and the Si film represents the transistor body. To operate the Ψ-MOSFET in situ (without lithography and metallization), low-pressure probes are placed on the silicon film and form source and drain point contacts.

Despite the device simplicity and nonparallelism of current lines, very pure MOSFET-like characteristics are produced. As shown in Figure 2, the simulated output I_DV_D is very similar to a classical MOSFET curve.

Positive or negative biases can be applied to the gate to form accumulation or inversion channels at the interface. For example a log I_D-V_G characteristic is shown for n-channel accumulation in Figure 3.

For all the reasons described above the Ψ-MOSFET stands as a unique method permitting a quick and complete evaluation of the electrical properties of SOI wafers prior to any device processing[1]. This article describes the use of 3-D numerical simulations which validate the method and show the optimum conditions for application and parameter extraction.

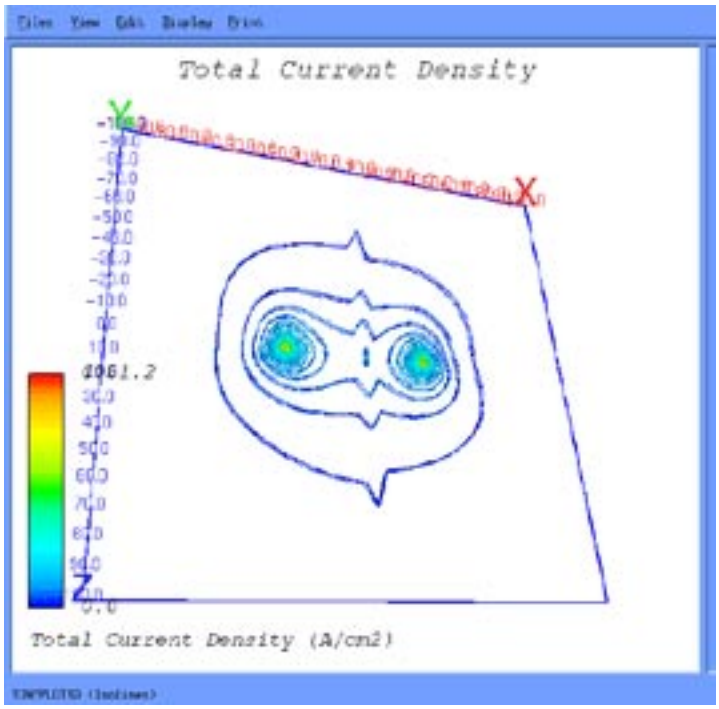

Figure 4. Current density lines (border-effect free structure) from **Device3D** simulation..

Structure Definition

The structure can be built either the internal syntax of **ATLAS** or **DevEdit3D** which allows interactive structure editing, structure specification and grid generation for 3D devices. The visualization of the structure is made with **TonyPlot3D** (Figure 4).

ATLAS is perfectly suited to this kind of simulation although it was developed for the simulation of fully processed devices. However special attention has to be paid the contact specification and especially to the determination of the work-function for the Schottky contact between the metal probe and the silicon film.

Simulation

ATLAS simulation calculates I_DV_G and I_DV_D characteristics for both inversion and accumulation channels in either n- or p-doped films (Figure 5). In addition, the simulations offer the distribution of the charge, potential (Figure 7) and electric field. The accuracy

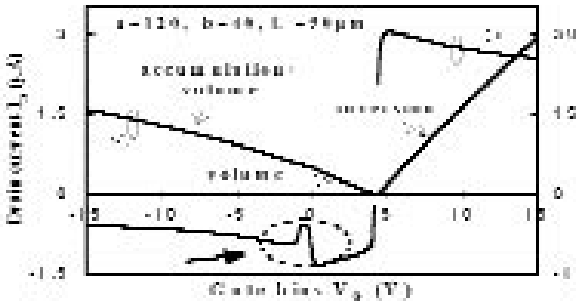

Figure 5. Simulated $I_D(V_G)$ and $gm(V_G)$.

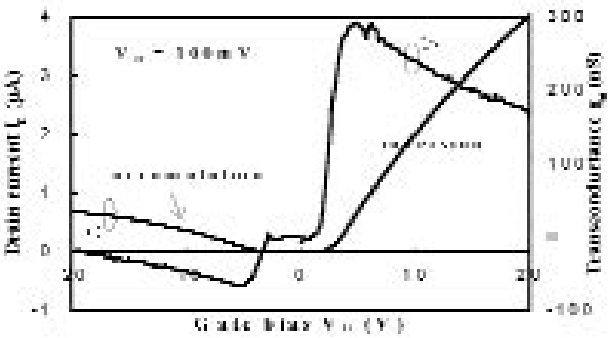

Figure 6. Experimental Ψ-MOSFET curves in a p-type UNIBOND

of the simulations has been validated by comparison with systematic experimental data (example in Figure 6) and by a self-consistent procedure: standard parameter extraction from the simulated curves and coherence of the output parameters with those initially fed into the simulator (carrier mobility, doping, oxide charges).

These simulations deliver illuminating information on the influence of several key parameters (film and substrate doping, film and buried oxide thickness, Schottky contact depth, series resistances, interface roughness).

More complex experimental situations have also been reproduced successfully:

- In a narrow range of gate voltages, a *depletion region* forms underneath the buried oxide. The depletion capacitance apparently modifies the oxide capacitance and gives rise to a hump in the drain current and tranconductance (dotted circle in Figure 5). This hump can be used to evaluate the substrate doping.
- In accumulation, the current flows not only at the interface but also in the *film volume*. The simulations allow to make distinction between these two components as a function of film doping and thickness.

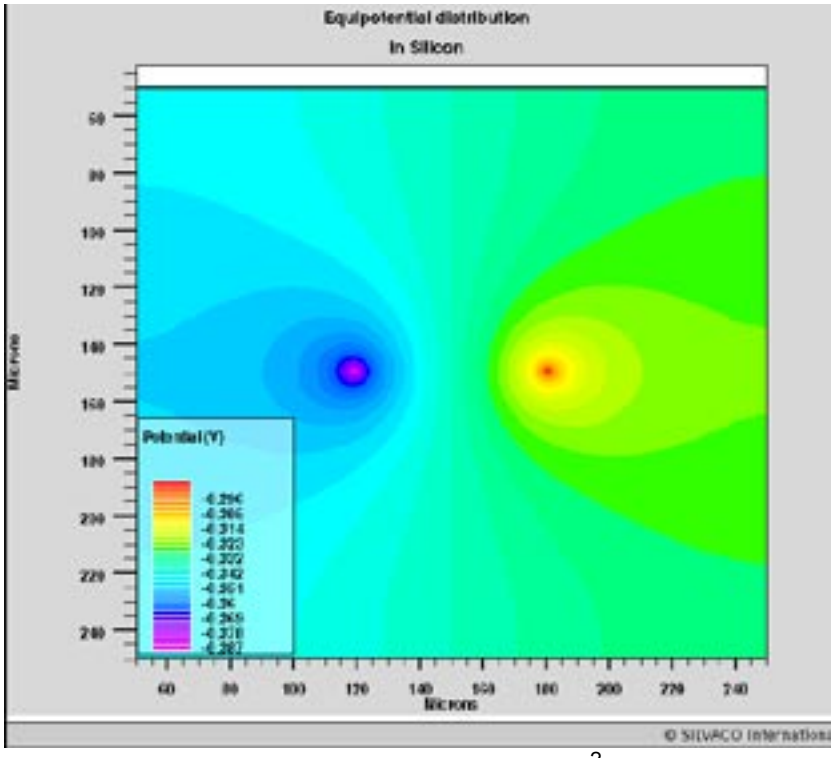

Figure 7. Equipotential line distribution in a 240x240μm^2 sample.

A practical concern with the Ψ-MOSFET technique is the *geometrical factor* f_g which replaces the transistor aspect ratio, W/L, and is not known a priori. This factor is estimated experimentally by the comparison between the Ψ-MOSFET and 4-point probe data [1]. Any uncertainty directly impacts on the extraction accuracy of the carrier mobility and threshold voltage.

3-D simulations do show the non-parallel current flow lines across the sample (Figure 4). We verified that, in samples large enough when compared to the probe interdistance, the geometrical factor is roughly $f_g \simeq 0.7$ in full agreement with the experiment.

A typical problem which can be sloved using 3-D simulations is the influence of the *sample size* and the *proximity* of the borders. The investigation was conducted by either shrinking the sample size or by placing the contacts closer

to the edges. In both cases, the resulting distortion of the field distribution (Figure 8) is responsible for an apparent degradation of the transconductance (Figure 9), and hence extracted mobility.

On the other hand, when the probe interdistance becomes comparable with the contact area (Figure 10) the short-channel/large-contact effect causes an over-estimation of the carrier mobility.

In order for the SOI material quality not to be underestimated or over estimated it is therefore necessary to respect certain rules in term of probe inter-distance on sample size.

Conclusion

The 3D simulator Device3D has reliably modeled the Ψ-MOSFET structure. The simulations have uncovered a number of non-obvious features of Ψ-MOS transistor behavior. This work makes clear the conditions required for reliable operation of the Ψ-MOSFET for SOI substrate characterization.

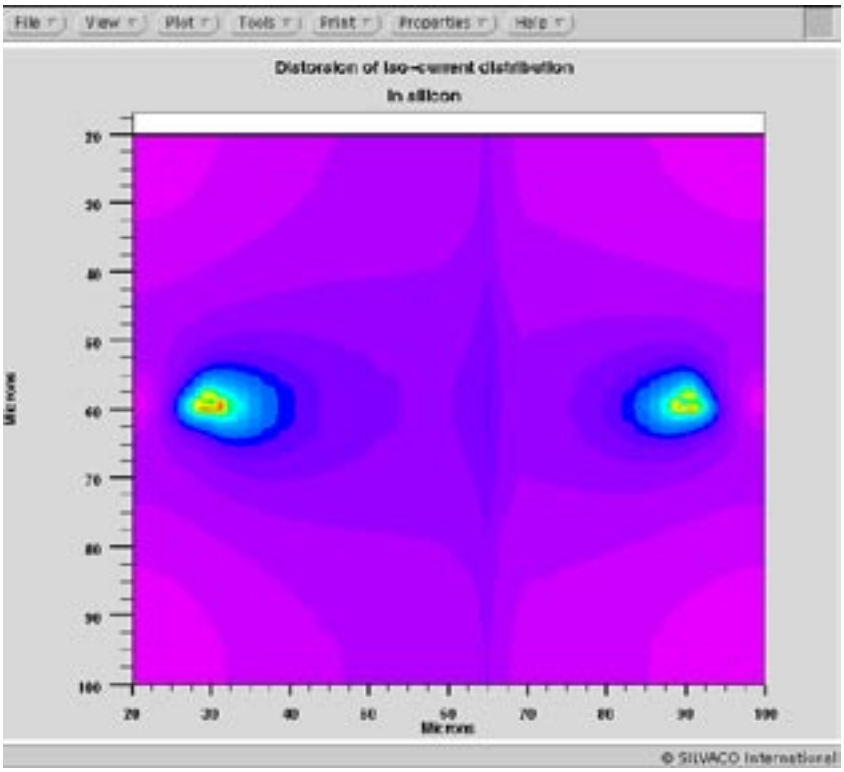

Figure 8. Border proximity effect shown by distortion of iso-current distribution.

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[1] S. Cristoloveanu, S. S. Li, Electrical Characterization of SOI Materials and Devices, Kluwer, (1995).

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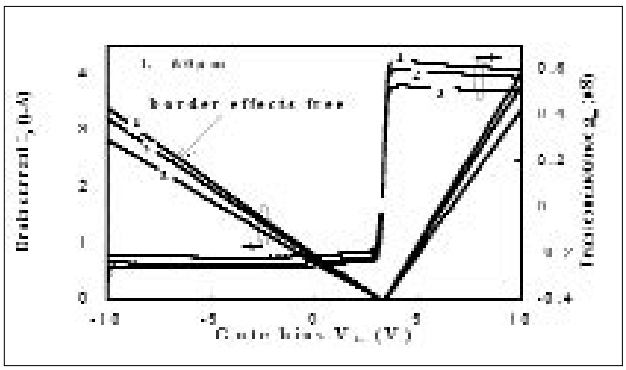

Figure 9. Simulated Ψ-MOSFET curves for different sample areas: (1) 200x200, (2) 120x120, (3) 80x80μm^2.

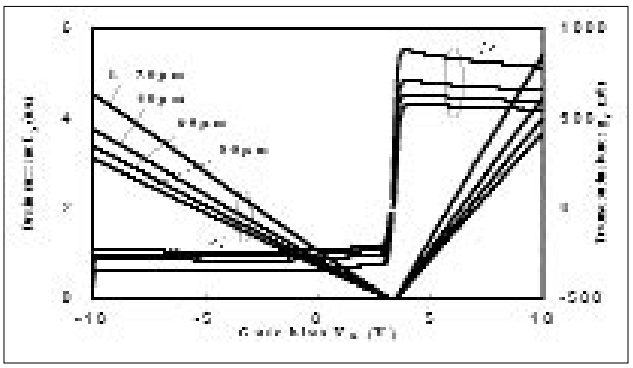

Figure 10. Influence of the 2-probe interdistance; 200x200μm2 sample, constant carrier mobility.

ATLAS Simulation of SiC Devices Using Anisotropic Mobility Models

Introduction

There has recently been a great deal of interest and research into using wide band gap materials, such as silicon carbide, in high power, high temperature applications. The operation of these devices has been found to be significantly different from the similar devices made using silicon. These differences are not fully explained by changing the material properties to those of SiC. Recent work has shown that the Hall mobilities in SiC are different depending on the crystalline axis where conduction is taking place [1]. This"anisotropic" mobility could dramatically affect device simulation results, particularly in power devices where current flow may be fully two-dimensional.

ATLAS has been modified so that this anisotropic mobility behavior may be modeled accurately as part of the device simulation. All of the existing mobility models implemented in **ATLAS** support this feature and only require the user to specify the mobility parameters in the two crystallographic planes used within the simulation. **ATLAS** then automatically accounts for the change in mobility as the vector of current flow moves through 360 degrees.

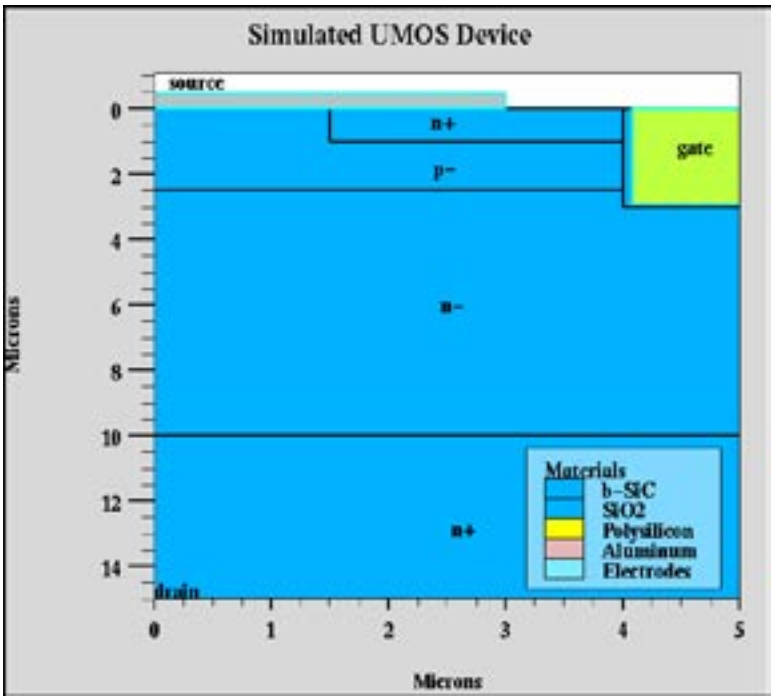

Figure 1. Structure of the trench-gated MOS device (UMOS) for simulation in **ATLAS.**

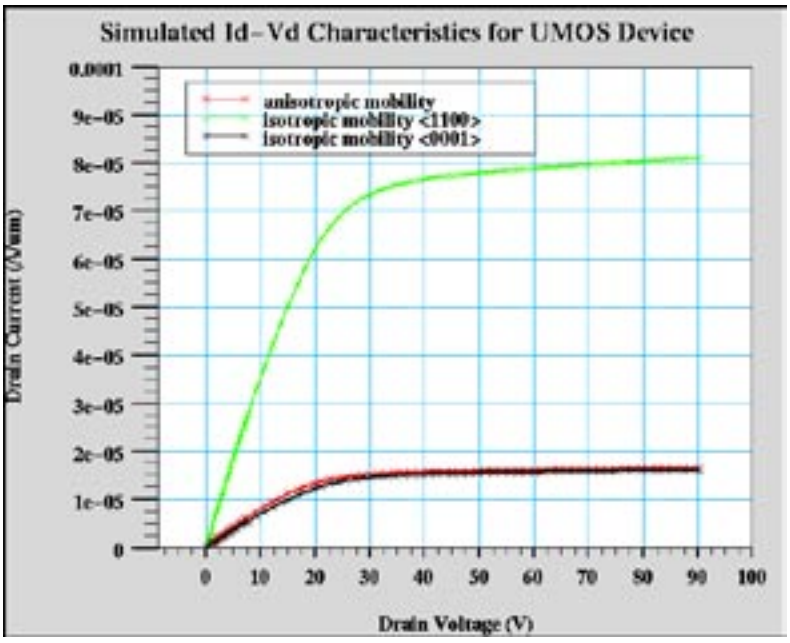

Figure 2. Simulation results of the Id-Vd characteristics of the UMOS device using isotropic and anisotropic mobility models. The anisotropic mobility results can be matched with one set of appropriate isotropic mobility coefficients.

To illustrate the effects that this model has on numerical simulation we have performed simulations on two 6H-SiC transistor structures - the trench gated MOS (UMOS) and the double implanted MOS (DIMOS) transistor[2] - with the standard physical material parameters suggested in [3]. The mobilities were defined for the planes <0001> and <1100> which resulted in a perpendicular to parallel mobility ratio of 5 as suggested by [4]. The plane <1100> contains the greater mobility values for both electrons and holes.

Simulation Results

Figure 1 shows the first structure to be simulated, the UMOS device. The Id-Vd characteristics of this device were simulated with both the standard isotropic and the anisotropic mobility models. The results of these simulations are shown in Figure 2. Two simulations were performed using the standard mobility model - firstly with the mobility coefficients for the plane <0001> and secondly with the mobility coefficients for the plane <1100>. As shown in the results the anisotropic mobility

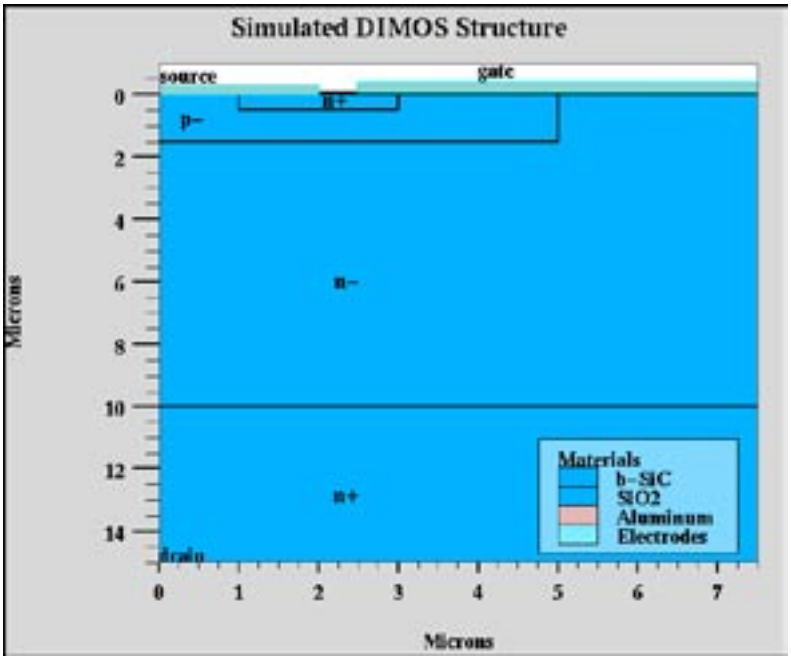

Figure 3. Structure of the double implanted MOS (DIMOS) device for simulation in ATLAS.

pinch-off region in the channel which lies in the<1100> plane. As a result the anisotropic model gives a higher on-resistance than the <1100> mobility but the saturation current will be close to that obtained for the <1100> plane but at a much higher drain voltage. The anisotropic model also results in a slightly different current flow path for the DIMOS device.

Figures 5 and 6 show the simulated current flowlines for the isotropic and anisotropic mobility models. The anisotropic model is shown to have a different current flow path. Firstly the current spreads out more in the n- region but is more dense around the corner of the p- region. This will affect both the series resistance and the self heating in the device.

model has given a similar characteristic to the isotropic model with mobility parameters of the <0001> plane. This result can be understood intuitively from Figure 1 as the current path is almost entirely in the <0001> plane. Also, the MOS channel, to the left of the gate, itself lies in the <0001> plane. The only current flow along <1100> will be in the n+ source region where there is only minimal resistance. As a result the mobility changes little along the current flow path and can be simulated using an isotropic mobility model.

Figure 3 shows the second device under analysis, the DIMOS device. The Id-Vd characteristics of this device were once again obtained with both the standard isotropic and the anisotropic mobility models, and are shown in Figure 4. In this device three different curves are obtained.The two curves obtained from the isotropic mobility model, for planes <0001> and <1100>, are both different to that obtained using the anisotropic mobility model. This difference is a result of the current flowing partly in the <0001> plane and partly in the <1100> plane. The MOS channel lies in the plane <1100>, which is the high mobility plane,whilst the majority of the distance over which the current flows is in the <0001> plane. Therefore the on-resistance, which is controlled by the <0001> plane, will be quite high. However current saturation is controlled by the

Conclusions

A new implementation of the mobility model into the semiconductor equations allows either isotropic or anisotropic mobility behavior tobe modeled. The implementation fully supports all the mobility models that are currently included in **ATLAS.** Two examples have been demonstrated. For a UMOS device the anisotopic mobility model was shown to correctly match the isotropic model. In the second example, the DIMOS device, the

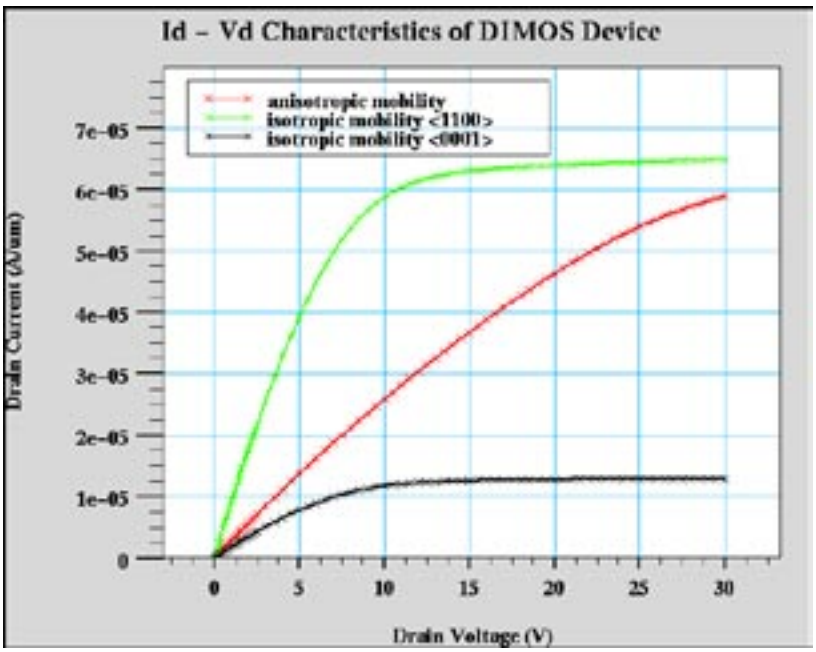

Figure 4. Simulation results showing the Id-Vd characteristics of the DIMOS device using both isotropic and anisotropic mobility models. The anisotropic results cannot be matched with just one set of isotropic mobility coefficients.

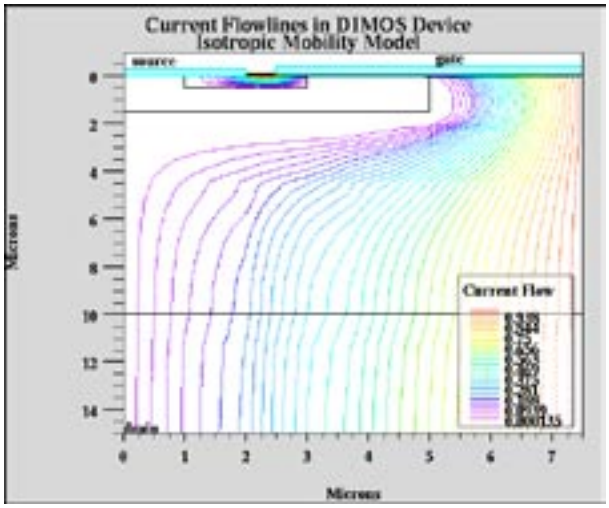

Figure 5. Two-dimensional plot of the current flowlines in the DIMOS device simulated with the isotropic mobility model.

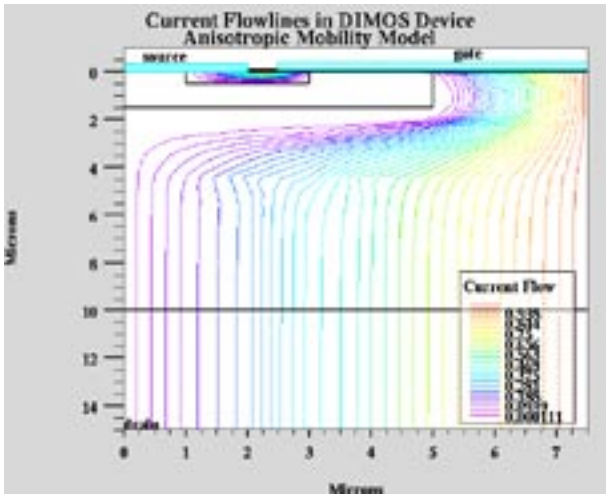

Figure 6. Two-dimensional plot of the current flowlines in the DIMOS device simulated with the anisotropic mobility model. The current spreading and current concentration with this model are different to those found with the isotropic mobility model.

complex two-dimensional current flow pattern can not be accurately modeled with the isotropic mobility model and only ananisotropic mobility model will yield the correct I-V characteristics.

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3D Simulation of Heterostructure Devices

Introduction

The three-dimensional silicon and GaAs device simulator **Device3D** has now been extended to allow simulation of heterostructure devices within the **ATLAS** framework. The new product **Blaze3D** includes the modeling of graded and abrupt heterojunction barriers which is critical to the simulation of important classes of devices such as HBTs and HEMTs.Two typical examples of the application of **Blaze3D** are presented here. Firstly, the collector avalanche breakdown of a SiGe base HBT is simulated. Secondly, a conventional GaAs-AlGaAs HEMT with a resistive T-gate is simulated in transient mode. The progression of a negative gate voltage pulse along the length of the gate is accompanied by the progressive turn-off of the channel conduction through the 2DEG in the GaAs.

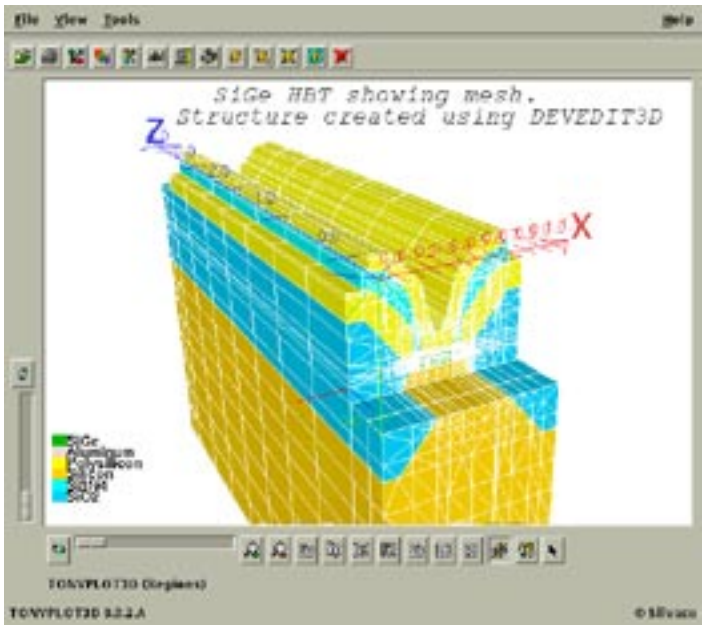

Figure 1. 3D super self aligned SiGe HBT structure created and meshed using **DevEdit3D.** Emitter and base contacts are polysilicon. A section of oxide isolation is removed from the view to reveal the confined SiGe base region with denser mesh.

Creation of Virtual Device Structures

3-dimensional structures may be created using **ATLAS** command syntax or more easily by using **DevEdit3D,** the 3D extension to the powerful **'De-**

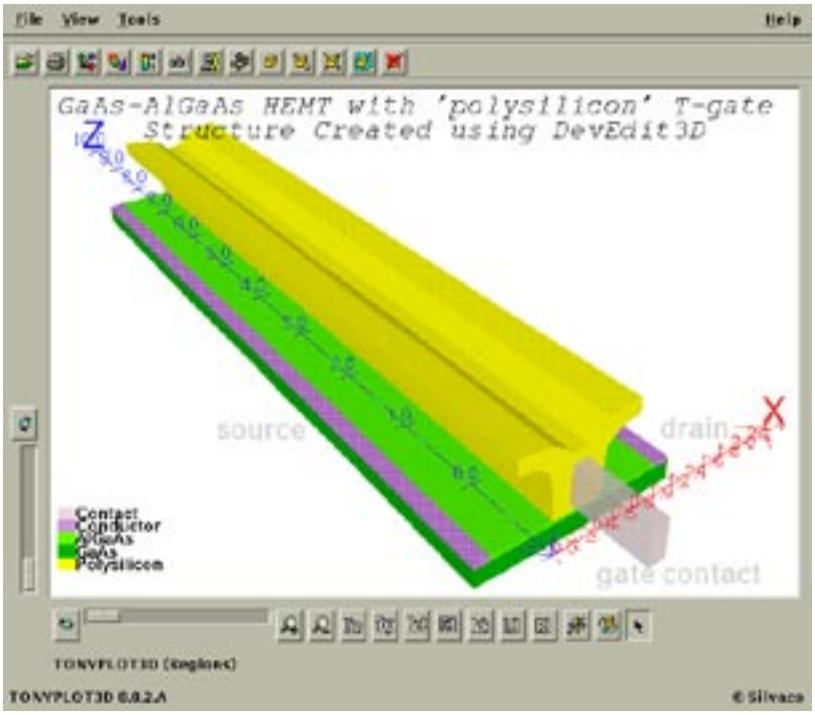

Figure 2. 3D AlGaAs-GaAs HEMT structure with resistive T-gate and end gate contact, from **DevEdit3D.**

vedit' device design and meshing package. **DevEdit3D** allows simulated or analytic doping profiles to be incorporated into device structures drawn on the screen and provides optimal 3D prismatic mesh generation based on user-defined constraints. The ability to automatically generate a conformal non-uniform mesh allows arbitrary device geometries to be studied. Concentration of mesh in active device regions, with relaxed mesh density elsewhere, helps minimize simulation times. A wide range of compound semiconductors are supported and layer composition fractions are easily defined.

Figure 1 shows a **TonyPlot3D** image of a 3D Si:SiGe HBT created using **DevEdit3D** and based on a device structure reported in[1]. The active device region is revealed by selectively removing a region of isolation oxide from the view. Concentration of the mesh in the confined SiGe base region may be noted.

A 3D HEMT structure (Figure 2) has the 10μm gate stripe extending along the z-axis with the channel conduction along the x-axis between source and drain. Because metals are treated as perfect conductors in **ATLAS**, the resistive gate is modeled by representing the gate metal as polysilicon with an appropriate resistivity and electron affinity.

Selection of Models

All the mobility models available in **Blaze** are incorporated in **Blaze3D**: concentration, transverse field and parallel field dependence (negative differential mobility or simple velocity saturation). **Blaze3D** also supports multiple recombination mechanisms (Auger, radiative and concentration dependent Schockley Read Hall) and band gap narrowing for simulation of bipolar transistors. Single event upset may be modeled as in **Device3D** and impact ionization may also be modeled to investigate breakdown limitations. **Blaze3D** carries the same comprehensive materials library as **Blaze**. This includes parameter defaults for more than 40 compound semiconductors. Arbitrary user-defined materials and properties are also supported. The SiGe HBT was simulated using the `AUGER`, `CONSRH`, `FLDMOB`, `CONMOB`, `BGN` and `IMPACT` models and biased into avalanche breakdown in the collector region under zero gate bias. For the simulation of the 3D HEMT, `FLDMOB` and `CONMOB` mobility models were invoked and single carrier mode was selected to reduce run time. The band offsets were set by defining the electron affinity of each layer. A -0.6V, 2pS gate voltage transient was applied to one end of the gate and the 2DEG channel observed to progressively turn off with time.

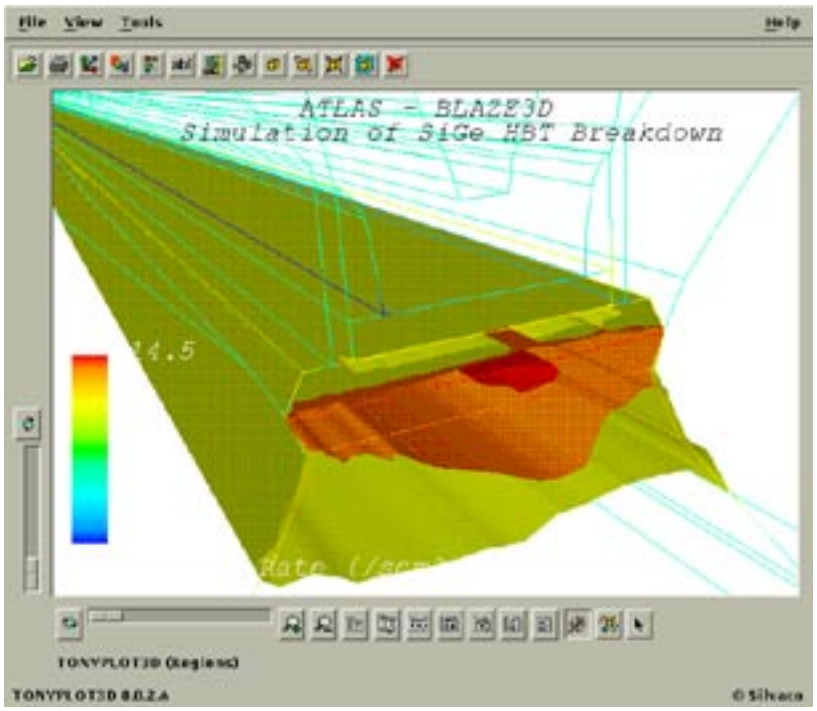

Figure 3. Isosurfaces of impact ionization rate reveal that the most intense avalanche multiplication is along the centre of the emitter stripe and in the n-doped SiGe collector region.

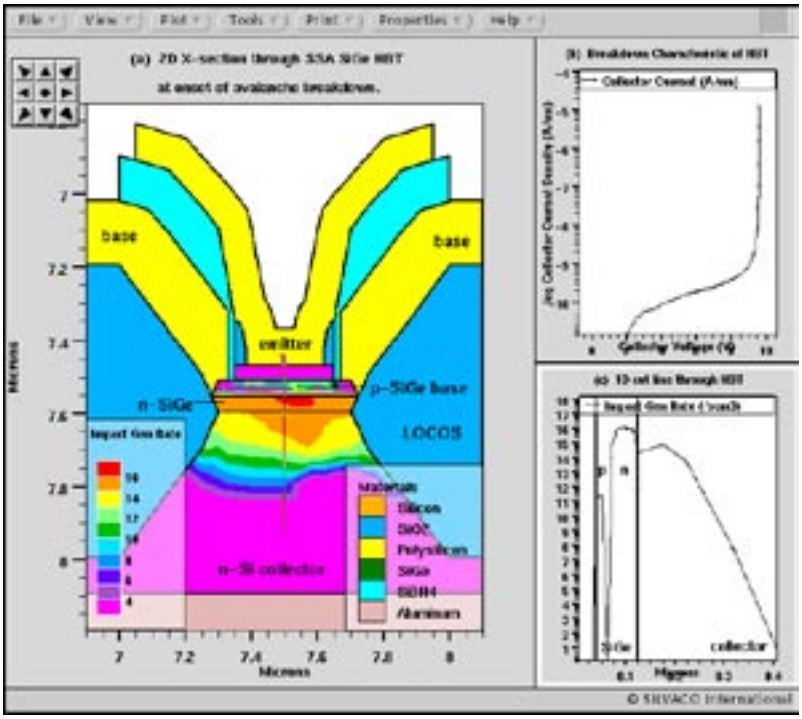

Figure 4. (a) cut plane through 3D HBT structure at onset of avalanche breakdown. Note the concentration of impact ionization in the centre of the n-SiGe collector extension region.(b) HBT collector breakdown characteristic. (c) cut line through 2D section showing graph of impact ionization rate with depth under poly emitter stripe.

Simulation Results

Results of device simulation are generally in the form of terminal current-voltage characteristics and 3D structure files. The latter may be viewed and analyzed using **TonyPlot3D** which provides advanced imaging and dissection capabilities. Taking the example of the HBT breakdown, the region of avalanche multiplication may be imaged as isosurfaces of impact generation rate (Figure 3). A 2D cut plane exported to **Tonyplot** (Figure 4a) gives a different perspective and a 1D cut line allows a graph to be drawn (Figure 4c). Figure 4b shows the breakdown characteristic. It may be observed in these plots that the avalanche breakdown in this HBT occurs primarily in the n-SiGe collector 'extension' region. The purpose of this layer is to avoid a potential barrier at the SiGe base -Si collector interface [1].

The response of the T-gated HEMT to a gate bias transient can be observed in Figure 5 which shows a 2D cut plane taken along the principal axis of the T-gate. The contours in the gate region represent the voltage which is clearly varying under the dynamic biasing as the gate is forced more negative (on the right side). The contours in the GaAs show the local electron channel current in the 2DEG and AlGaAs is consistent with the gate potential, being lower on the right hand side where the gate potential is more negative.

Conclusion

Blaze3D extends **ATLAS** simulation capability to include arbitrary three-dimensional heterostructure devices. Combined with **DevEdit3D** and **TonyPlot3D,** accurate structure definition and results analysis are possible for 3D device technology development. These features are demonstrated for typical examples of HBT and HEMT.

Reference

[1] A. Pruijboom et. al. IEDM 95-747 (1995).

NOTE: *Full color graphics of the 3D hetrostructures may be viewed at: www.silvaco.com*

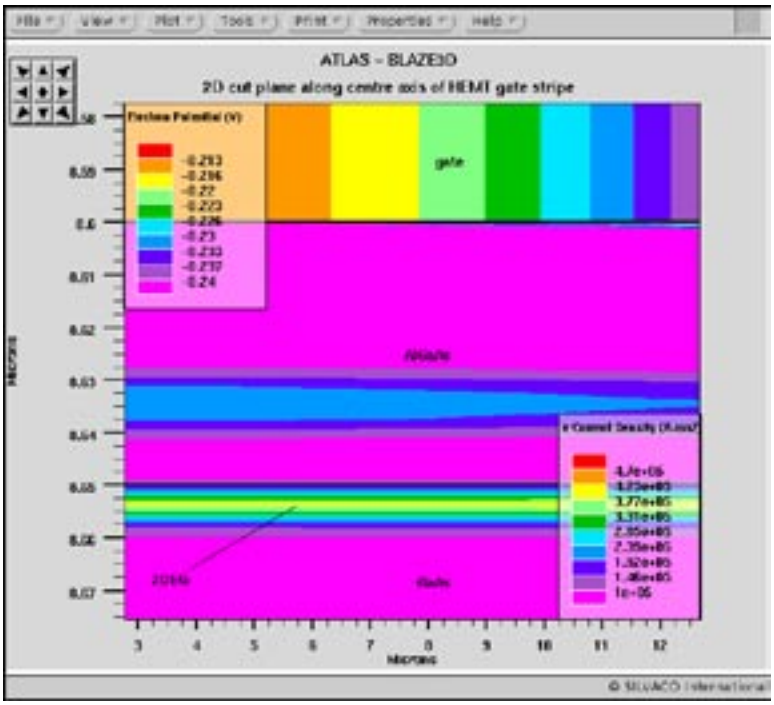

Figure 5: 2D cut plane taken from a **Blaze3D** solution for the 3D HEMT during a negative gate bias transient. The section is along the major axis of the resistive T-gate and shows the potential gradient along its length. The channel conduction (particularly the parasitic conduction in the AlGaAs) is consistent with the gate potential profile.

Calendar of Events

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11	ICCAD'97, Santa Clara
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December

1	MRS Meeting, Boston
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Bulletin Board

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Silvaco will be demonstrating the latest advances in our **Virtual Wafer Fab** TCAD simulation products at the conference which will be held at the Washington D.C. Hilton on December 7-10, 1997. Silvaco's demo suite will be located in Suite C325 on the Lobby floor. All conference participants are welcome to come and see the exciting new tools available from Silvaco including: **FastAtlas** - an extremely fast FET device simulator, **Blaze3D** - a 3D device simulator for compound materials, and **CLEVER** - highly accurate cell level LPE based on Silvaco's advanced 3D process simulation capabilities. All participants are encouraged to take advantage of this opportunity to come and see how the only significant remaining commercial TCAD vendor can help meet your technology development needs.

Silvaco at MRS Fall Meeting!

Dr. Misha Temkin will present a paper showing the latest enhancements to **ATHENA** entitled "Computationally Efficient Model for 2D Ion Implantation Simulation" at the "Semiconductor Process and Device Performance Modeling Symposium" during Material Research Society 1997 Fall Meeting, December 1st - 5th in Boston, Ma.

Taiwan Workshops

Our new Hsinchu office is now open and will start providing regular workshops for Taiwan customers. The first two workshops are titled: "Advanced diffusion models in ATHENA" for TCAD users, and "**SmartSpice** BSIM3v3 Capacitance Modeling and AC Parameters Extraction using **UTMOST**" for **UTMOST** users.

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

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Hints, Tips and Solutions

Andy Strachan, Applications and Support Manager

Q: How is the coupling ratio between the floating gate and control gate of a Flash EEPROM modeled in ATLAS?

A: In EEPROM devices the floating gate is capacitively coupled to the control gate and the substrate. The exact ratio of the coupling is determined by the relative shape of the floating and control gate electrodes as well as the inter-gate layer thicknesses. For most structures full 3D simulations would be required to model the control and floating gate geometries correctly. Although **ATLAS/ Device3D** can perform simulations of 3D Flash memory structures it is often more convienient to find a solution using 2D simulation.

By default, in 2D simulations the coupling capacitances between the floating gate and the control gate and other electrodes is determined only by the layer thicknesses and other 2D geometries. However **ATLAS** enables the user to specify an extra capacitance between a floating electrode and any other electrode in the device structure. Most commonly this is an extra capacitance between the floating gate and the control gate. This would be defined using the syntax:

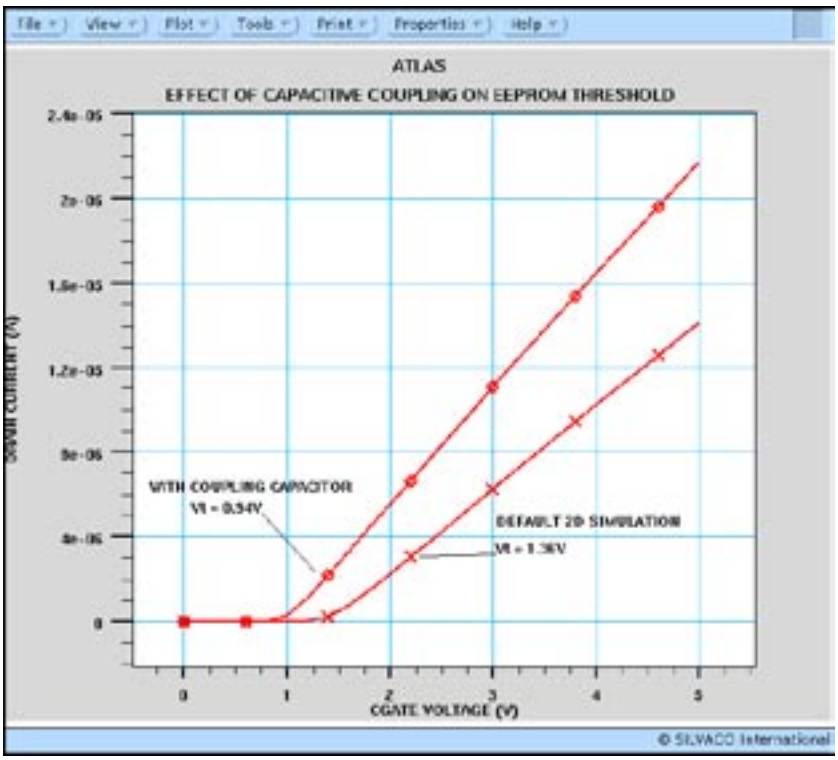

Figure 1. Correct setting of the coupling ratio is required for accurate EEPROM threshold simulation.

```
CONTACT          NAME=FGATE    FLOATING
EL1.CAP=CGATE FG1.CAP=<value>
```

Users should note this capacitance is applied between electrode nodes. This differs from the usual lumped capacitance definition on the `CONTACT` statement which applies between the specified electrode and ground.

The effect of the extra capacitance is to give the correct coupling ratio seen in simple EEPROM simulations such as the threshold voltage evalution shown in Figure 1. Generally the value of the external capacitor should be tuned to the threshold behavior before more complex simulations of programming, erasing or breakdown are done.

Capacitive coupling between the floating gate and other electrodes can also be modeled by additional syntax. The syntax `ELx.CAP` and `FGx.CAP`, where `x`=1 to 4, can be used to define up to four different electrode names and capacitors .

Q: How can EEPROM devices be simulated in a circuit environment using ATLAS/MixedMode?

A: Any type of EEPROM or non-volatile memory from **ATLAS** can be embedded in a SPICE circuit and simulated using **MixedMode.** The **ATLAS** device should be defined in the circuit netlist using syntax such as:

```
AEPR -1=FGATE 1=CGATE 2=DRAIN 0=SUBSTRATE 0=SOURCE \
WIDTH=<value> INFILE=<filename>
```

Note that the floating gate is assigned a negative node number. This allows **ATLAS** to store the change on the floating gate during **MixedMode** simulations.

In the numerical device parameter definition of the **MixedMode** input file the floating gate should still be defined as a floating electrode using the `CONTACT` statement. The coupling capacitances described above should also be defined using the `CONTACT` statement and the syntax refered to in the previous question. Users should not make any connection to the floating gate node in the SPICE circuit. This especially includes

capacitors between the floating gate and any node. This is due to the difference in definition of a floating node in SPICE and a floating gate in **ATLAS.**

Programming and Erasing simulations in a circuit environment can be performed using **ATLAS/ MixedMode.** Figure 2 shows a **Flash** programming simulation where the EEPROM device is in series with a MOS transistor simulated in SPICE. To highlight **MixedMode** usage the comparison shows the effect of variations in the series MOSFET on the programming curve.

Q: How can 'one-shot' EEPROM programming be modeled with ATLAS?

A: **ATLAS** can model the one-shot programming by mirroring the test conditions used in measurements. In this test the control gate of Flash memory device is held at a high voltage. Then the drain is ramped up from zero to a voltage around breakdown.

During the V_{DS} ramp, at around 2-3V hot electron gate current programs the floating gate causing a V_T shift. This causes the drain current to drop and hot electron current to fall off.

If a DC solution was used in **ATLAS** the results would be incorrect since the connection between injected gate current and floating gate charge is only possible if the time scale is known. Thus transient simulation should be used in **ATLAS.** The length of the transient needs to be matched to the 'one-shot' programming measurement setup.

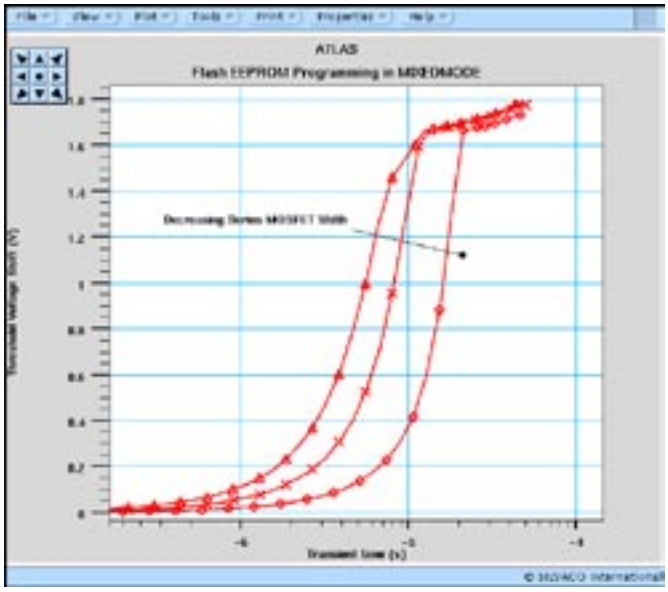

Figure 2. EEPROM programming simulated in **MixedMode.** Variation in parameters of the series MOSFET is used to illustrate the effect of circuit variation.

However since the timescale of the drain voltage ramp is typically slow the device is in equilibrium at each time step. **ATLAS** includes a special numerical technique to deal with this situation defined by:

```
METHOD QUASISTATIC
```

This quasistatic method adjusts the error control within **ATLAS** to avoid excessively short timesteps. It is relevant for all other types of quasistatic transient simulations.

Although the simulation is run as a transient mode the final results are displayed as an I_D/V_{DS} curve (Figure 3). The curve clearly shows the on-set of programming and the final punchthough.

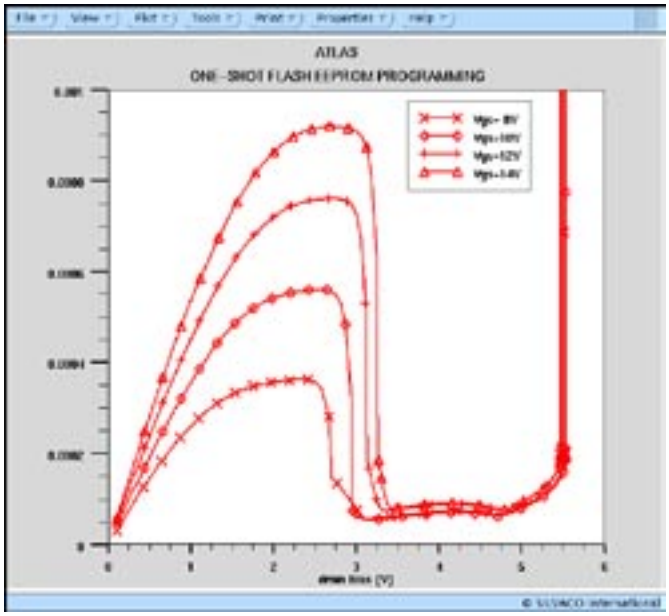

Figure 3. 'One-shot' programming characteristic of a Flash Memory device is simulated by using quasi-static transient simulation in **ATLAS.**

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